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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/748,947
Filing Date: December 27, 2000
Appellant(s): DUMONT ET AL.

Jorge Tony Vilabon
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 08/03/2006 appealing from the Office action mailed 01/11/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,371,551	Logan	12-1994
6,317,164	Hruseeky	11-2001
6,614,984	Rigatti	09-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 11-23, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Logan (US Pat. No. 5,371,551) in view of Hrusecky (US Pat. No. 6,317,164).

Regarding claims 11 and 17, Logan discloses a digital video system using concurrent recording and playback, comprising:

an encoder of a first analog signal into a first digital stream (see Fig.1, 4B and 4C; col. 3 lines 8-11; col. 4 line 14-25);

a decoder of a second digital stream into a second analog signal (see Fig.1, Decompressor 8; col. 3 line 20-27);

a medium interface for reading and recording on a medium (see Fig.1 memory system 5; col.3 line 16-20);

at least one digital source outputting a third digital stream (see Fig.1 RF tuner 4A see col.3 line 60-63);

a multiplexer coupled to the encoder and to the decoder and to the digital source and to the medium interface (see Fig.1 a switching node 3 col.3 line 8-11). It is inherent that

the multiplexer must comprise a first switch, which selectively couples the decoder to the encoder or to the digital source. Claim 1 differs from Logan in that the claim further requires wherein the multiplexer comprises a first switch, which selectively couples the decoder directly to the encoder or to the digital source such that the first digital stream from the encoder is able to be communicated to the decoder without prior recording.

In the same field of endeavor, Hrusecky discloses the multiplexer (see selecting switch (25) comprises a first switch, which selectively couples the decoder (see digital video decoder (27) directly to the encoder or to the digital source such that the first digital stream from the encoder is able to be communicated to the decoder without prior recording (see col. 3 line 64-col. 4 line 38). Hrusecky further discloses sources (see fig. 1 (11, 12, 14) are provided satellite, CD, ROM, or DVD disk or combinations of various sources (see col. 4 lines 10-17). Hrusecky further discloses the sources are encoded in accordance with MPEG standard (see col. 4 lines 1-9 and lines 24-30). Hrusecky further discloses frame buffer (see fig. 1 buffer (28) and display screen (29)) stores frame and the display screen displays frames stored in the buffer (see col. 4 lines 61-66). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Logan by providing a decoder directly coupled to the source in order to decode a plurality of digital video data streams using a single decoder.

Regarding claims 12 and 18, Logan shows in figure 1 the multiplexer (the switching node 3), which selectively couples the medium interface (memory system 5) to the encoder (input signal processing unit 12). It is inherent that the switching node (3)

comprises a second switch which selectively couples the memory system (5) to the input signal processing unit (12).

Regarding claims 13, 16, and 19, Logan shows that the switching node(3) selectively couples the decoder (see Fig.1, Decompressor 8 col. 3 line 20-27) to the encoder(see Fig.1, 4B and 4C col. 3 lines 8-11; col. 4 line 14-25), to the digital source, (see fig.1 RF tuner 4A and col.3 line 60-63), to the transcoder(see fig.1 compressor, 4D and col. 3 line 68-70) or to the medium interface(memory system 8; see col.3 line 25-28).

Regarding claim 14, Logan teaches a transcoder receiving a fourth digital stream is coupled to the multiplexer (see fig.1 compressor 4D, and col. 3 line 69).

Regarding claim 15, Logan shows in Fig.1 that the second switch (the switching node 3) connects the medium interface (see fig.1, memory system 5) to the encoder (see fig. 1 the compressed RF tuner 4B and 4C), to the digital source (see fig.1 4A) or to the transcoder (see fig. 1 compressor 4D).

Regarding claims 20 and 22, Logan teaches that the digital encoder coupled to a tuner for receiving analog signals (see col. 3 line 60-63).

Regarding claim 21, limitations in claim 21 can be found in claim 11 above. Therefore, claim 21 is analyzed and rejected as previously discussed with respect to claims 11. It is noted that the Logan discloses a medium interface for reading a second digital stream from a medium (see fig. 1 (5) and col. 3 lines 11-24). Logan further discloses a decoder for decoding the first digital stream or the second digital stream into a second analog stream (see fig. 1 and col. 3 lines 1-27).

Regarding claim 23, Logan teaches that the second analog signal is sent to a display (see col. 3 line 20 and fig. 1 where it shows output from (8) to (10)).

Regarding claim 25, Logan teaches means for allowing the first digital stream (see fig. 1. RF tuner 4A in box 12, input signal processing unit) to be recorded on the medium by the medium interface (fig.1, memory 5 see col.3 line 24-27).

Regarding claim 26, Logan teaches in figure 1 a second switch (switching node 3) has an input connected to the encoder (signal processing unit 12) and an output connected to the medium interface (memory system 5).

3. Claims 11, 17, 21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rigatti (US Pat. No. 6, 614,984) in view of Hrusecky (US Pat. No. 6,317,164).

Regarding claim 11, Rigatti discloses a digital video recorder comprising an encoder of a first analog signal into a first digital stream (see fig.5, A/D (5) and col. 3 lines 49-51. The A/D converts the first analog signal into first digital stream); a decoder of a second digital stream into a second analog signal (see fig. 5 analog output (8) and input/ output port (12) and col. 4 lines 3-12); a medium interface for reading and recording on a medium (see fig. 5 memory (1) and col. 3 lines 38-47); at least one digital source outputting a third digital stream (see col. 3 lines 47-49 and fig. 5 digital input (15)); and a multiplexer coupled to the encoder and to the decoder and to the digital source and to the medium interface (see fig. 5 switch (14), is coupled to the A/D (5), Input/output port (12), D/A (18), memory (1), and col. 3 lines 48-64 and col. 4 lines 3-12), the multiplexer comprises a first switch, which selectively couples the decoder to

the encoder or to the digital source (see col. 3 line 65-col. 4 line 20). Claim 1 differs from Logan in that the claim further requires wherein the multiplexer comprises a first switch, which selectively couples the decoder directly to the encoder or to the digital source such that the first digital stream from the encoder is able to be communicated to the decoder without prior recording.

In the same field of endeavor, Hrusecky discloses the multiplexer (see selecting switch (25) comprises a first switch, which selectively couples the decoder (see digital video decoder (27) directly to the encoder or to the digital source such that the first digital stream from the encoder is able to be communicated to the decoder without prior recording (see col. 3 line 64-col. 4 line 38). Hrusecky further discloses sources (see fig. 1 (11, 12, 14) are provided satellite, CD, ROM, or DVD disk or combinations of various sources (see col. 4 lines 10-17). Hrusecky further discloses the sources are encoded in accordance with MPEG standard (see col. 4 lines 1-9 and lines 24-30). Hrusecky further discloses frame buffer (see fig. 1 buffer (28) and display screen (29)) stores frame and the display screen displays frames stored in the buffer (see col. 4 lines 61-66). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Logan by providing a decoder directly coupled to the source in order to decode a plurality of digital video data streams using a single decoder.

Regarding claim 17, limitations in claim 17 can be found in claim 11 above. Therefore, claim 17 is analyzed and rejected as previously discussed with respect to claims 11. It is noted that the Rigatti discloses a digital video recorder comprising a

digital encoder (see col. 3 lines 49-51 and fig. 5 A/D (5)). Rigatti further discloses a digital decoder (see col. 4 lines 3-12 and see fig. 5 analog output (18) and input/ output port (12)); a medium interface for reading and recording on a medium (see fig. 5 memory (1) and col. 3 lines 38-47); a multiplexer (switch 14 in fig. 5) coupled to the encoder and to the decoder and to the digital source and to the medium interface (see fig. 5 switch (14), is coupled to the A/D (5), Input/output port (12), D/A (18), memory (1), and col. 3 lines 48-64 and col. 4 lines 3-12), the multiplexer having a first switch which couples the digital decoder to the digital encoder (see col. 3 line 65-col. 4 line 20).

Regarding claim 21, limitations in claim 21 can be found in claim 11 above. Therefore, claim 21 is analyzed and rejected as previously discussed with respect to claims 11. It is noted that the Rigatti discloses a medium interface for reading a second digital stream from a medium (see col. 3 line 45-col. 4 line 12 of Rigatti).

Regarding claim 24, Rigatti discloses a first switch (see output from A/D (5) and input to switch (14) in fig. 5) has a first input connected to the encoder (see col. 3 lines 49-54), a second input connected to the medium interface (see input from second format controller (4) in fig. 5 and col. 4 lines 13-20) and an output connected to the decoder (see analog output (18), D/A (6), or input/output port (12) in fig. 5 and col. 4 lines 6-12).

(10) Response to Argument

I. Regarding claims 11-23, 25 and 26, in re page 17 the Appellant states "There is absolutely no motivation or suggestion in either reference for the combination of the references to attempt to teach the invention of the Appellant. More specifically, there is

no motivation or suggestion in the invention of Logan for the combination of the references and likewise, the invention of Hrusecky does not expressly or impliedly motivates or suggest such a combination as required for the combination of references under 35 U.S.C. § 103."

In response the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the cited primary reference, Logan, discloses a decompressor 8 (see fig. 1 of Logan) to decode the recorded information prior to display. The recorded information are one or more previously received signals which are supplied by the input unit 4, where the input unit includes encoders (see fig. 1 of Logan). Logan teaches decoding the incoming signals (encoded signals) after recording. However the present Application claim 11 cites decoding the signals prior to recording. In the same field of endeavor Hrusecky discloses a plurality of incoming signals are encoded prior to recording in the frame buffer 28 (see fig. 1). Hrusecky further teaches these incoming signals are encoded in accordance with MPEG standard (see col. 4 lines 1-9 and lines 24-30 and fig. 1). Hrusecky uses a single decoder to create multiple scaled videos. The digital video decoder 27 includes a downscaling function for generating a reduced size or downscaled frame prior to recording (see col. 4). The digital video decoder 27 also

includes an OSD (on screen display) processor which can scale the size of an MPEG video presentation while displaying multiple previously scaled single frames. Therefore decoding a plurality of digital video stream using a single decoder as noted earlier in the prior art considerations would have also been an adequate motivation.

In re page 18 the Appellant states, "Logan fails to teach, suggest or make obvious at least that the multiplexer comprises a first switch, which selectively couples the decoder directly to the encoder or to the digital source such that the first digital stream from the encoder is able to be communicated to the decoder without prior recording as taught in the Appellant's Specification and claimed by at least the Appellant's independent claim 11."

In response the Examiner respectfully disagrees. Logan discloses a multiplexer (switching node 3 in fig. 1) where one or more incoming video signals are combined. The incoming video signals are processed by the encoders (compressors in the doted rectangle 12 in fig. 1). The switching node 3 selects or switches one of the incoming signals and output the selected signals to the memory sub system 5. The switching node performs switching function in order to select one of the incoming signals. The switching node 3 of Logan couples the decoder to the encoder after recording. In the same field of endeavor Hrusecky discloses a plurality of incoming signals are encoded prior to recording in the frame buffer 28 (see fig. 1). Hrusecky uses a single decoder to create multiple scaled videos. Hrusecky discloses the multiplexer (see selecting switch (25) comprises a first switch, which selectively couples the decoder (see digital video decoder (27) directly to the sources prior to recording (see col. 3 line 64-col. 4 line 38).

Hrusecky further discloses sources (see fig. 1 (11, 12, 14) are provided satellite, CD, ROM, or DVD disk or combinations of various sources (see col. 4 lines 10-17). Hrusecky further discloses the sources are encoded in accordance with MPEG standard (see col. 4 lines 1-9 and lines 24-30). Hrusecky further discloses frame buffer (see fig. 1 buffer (28) and display screen (29)) stores frame and the display screen displays frames stored in the buffer (see col. 4 lines 61-66).

Therefore when the teaching of Logan and the teaching of Hrusecky combines as proposed by the examiner the decoder of Hrusecky would be directly connected to the encoder of Logan. Logan teaches, suggests or make obvious at least that the multiplexer (switching node 3 which switches the input signals coming out from box 12 see fig. 1 in Logan) comprises a first switch, which selectively couples the decoder (decoder 27 Hrusecky) of directly to the encoder or to the digital source such that the first digital stream from the encoder is able to be communicated to the decoder without prior to recording.

In response to Appellant's argument that the references fail to show certain features of appellant's invention, it is noted that the features upon which appellant relies (i.e., in re page 19 the Appellant states "The multiplexer 3 and 25 disclosed by both Logan and Hrusecky only comprises a single output." a multiplexer having two outputs) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

II. Regard to claims 11, 17, 21 and 24, in re page 35 the Appellant states "Rigatti teaches a digital video system including almost all of the elements of the Appellant's claims but that the Appellant's claim 11 differs from Rigatti in that the claims further require wherein the multiplexer comprises a first switch, which selectively couples the decoder directly to the encoder or to the digital source such that the first digital stream from the encoder is able to be communicated to the decoder without prior recording. The Appellant respectfully agrees that Rigatti fails to teach at least the above identified limitation of at least the Appellant's claim 11."

In response the Examiner respectfully disagrees. Rigatti discloses a digital video recorder comprising an encoder of a first analog signal into a first digital stream (see fig.5, A/D (5) and col. 3 lines 49-51. The A/D converts the first analog signal into first digital stream); a decoder of a second digital stream into a second analog signal (see fig. 5 analog output (8) and input/ output port (12) and col. 4 lines 3-12); a medium interface for reading and recording on a medium (see fig. 5 memory (1) and col. 3 lines 38-47); at least one digital source outputting a third digital stream (see col. 3 lines 47-49 and fig. 5 digital input (15)); and a multiplexer coupled to the encoder and to the decoder and to the digital source and to the medium interface (see fig. 5 switch (14), is coupled to the A/D (5), Input/output port (12), D/A (18), memory (1), and col. 3 lines 48-64 and col. 4 lines 3-12), the multiplexer comprises a first switch, which selectively couples the decoder to the encoder or to the digital source (see col. 3 line 65-col. 4 line 20). Claim 11 differs from Logan in that the claim further requires wherein the multiplexer comprises a first switch, which selectively couples the decoder directly to the

encoder or to the digital source such that the first digital stream from the encoder is able to be communicated to the decoder without prior recording.

The secondary reference of Hrusecky discloses the multiplexer (see selecting switch (25) comprises a first switch, which selectively couples the decoder (see digital video decoder (27) directly to the encoder or to the digital source such that the first digital stream from the encoder is able to be communicated to the decoder without prior recording (see col. 3 line 64-col. 4 line 38). Hrusecky further discloses sources (see fig. 1 (11, 12, 14) are provided satellite, CD, ROM, or DVD disk or combinations of various sources (see col. 4 lines 10-17). Hrusecky further discloses the sources are encoded in accordance with MPEG standard (see col. 4 lines 1-9 and lines 24-30). Hrusecky further discloses frame buffer (see fig. 1 buffer (28) and display screen (29)) stores frame and the display screen displays frames stored in the buffer (see col. 4 lines 61-66).

Therefore Rigatti teaches the multiplexer (switch 14 in Rigatti) comprises a first switch, which selectively couples the decoder directly to the encoder (see selecting switch in Hrusecky) or to the digital source such that the first digital stream from the encoder is able to be communicates to the decoder without prior recording.

In response to Appellant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re*

Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the digital video decoder 27 includes a downscaling function for generating a reduced size or downscaled frame prior to recording (see col. 4). The digital video decoder 27 also includes an OSD (on screen display) processor which can scale the size of an MPEG video presentation while displaying multiple previously scaled single frames in order to perform accelerated decoding process.

Therefore a reference must be considered not only for what it expressly teaches, but also for what it fairly suggests. In our view, the artisan would have recognized the obviousness of connecting the encoder directly to the decoder prior to recording.

For the above reasons, it is believed that the rejection should be sustained.

(11) Evidence Appendix

No evidence entered and relied upon in the Appeal.

(12) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Helen Shibru

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